CLAIMS

WE CLAIM:

1. A method of measuring the level of a recurring data signal at selected times relative to a recurring reference associated with the data signal, the method comprising the steps of:

   (a) comparing the instantaneous voltage of a clock signal associated with the data signal to a clock threshold voltage to produce a logical clock signal;

   (b) delaying the logical clock signal by a selected first amount to produce a delayed logical clock signal;

   (c) comparing the instantaneous voltage of the data signal to be measured to a first data threshold voltage to produce a first logical data signal;

   (d) delaying the first logical data signal by a selected second amount to produce a first delayed logical data signal;

   (e) delaying the delayed logical clock signal by a selected third amount to produce a doubly delayed logical clock signal;

   (f) capturing the value of the first delayed logical data signal in response to the delayed logical clock signal;

   (g) capturing the value of the first delayed logical data signal in response to the doubly delayed logical clock signal;

   (h) generating the XOR of the value captured in step (f) and the value captured in step (g);

   (i) comparing the instantaneous voltage of the data signal to be measured to a second data threshold voltage to produce a second logical data signal;

   (j) delaying the second logical data signal by the selected second amount to produce a second delayed logical data signal;

   (k) capturing the value of the second delayed logical data signal in response to the delayed logical clock signal;

   (l) generating the XOR of the value captured in step (f) and the value captured in step (k);

(m) generating the OR of the XOR values generated in steps (h) and (l); and

(n) capturing the logical value of the OR operation generated in step (m).

2. A method as in claim 1 further comprising the steps of:

(o) repeating steps (a) through (n) until a selected condition is satisfied;

(p) subsequent to step (o), storing, in a data structure indexed according to a difference between the first and second amounts and also indexed according to one of the first and second data threshold voltages, a count representing the number of times the captured value of step (n) is TRUE during the repeating of steps (a) through (n);

(q) repeating steps (a) through (p) with identically altered values for the first and second data threshold voltages in combination with altered values for the second amount; and

(r) generating an eye diagram from the counts stored in the data structure.

3. A method of measuring the level of a recurring data signal at selected times relative to a recurring reference associated with the data signal, the method comprising the steps of:

(a) comparing the instantaneous voltage of a clock signal associated with the data signal to a clock threshold voltage to produce a logical clock signal;

(b) delaying the logical clock signal by a selected first amount to produce a delayed logical clock signal;

(c) comparing the instantaneous voltage of the data signal to be measured to a first data threshold voltage to produce a first logical data signal;

(d) delaying the first logical data signal by a selected second amount to produce a first delayed logical data signal;

(e) delaying the delayed logical clock signal by a selected third amount to produce a doubly delayed logical clock signal;

(f) capturing the value of the first delayed logical data signal in response to the delayed logical clock signal;

(g) capturing the value of the first delayed logical data signal in response to the doubly delayed logical clock signal;

(h) generating the XOR of the value captured in step (f) and the value captured in step (g);

(i) comparing the instantaneous voltage of the data signal to be measured to a second data threshold voltage to produce a second logical data signal;

(j) delaying the second logical data signal by a selected fourth amount to produce a second delayed logical data signal;

(k) capturing the value of the first delayed logical data signal in response to the delayed logical clock signal;

(l) generating the XOR of the value captured in step (f) and the value captured in step (k);

(m) generating the OR of the XOR values generated in steps (h) and (l); and

(n) capturing the logical value of the OR operation generated in step (m).

4. A method as in claim 3 further comprising the steps of:

(o) repeating steps (a) through (n) until a selected condition is satisfied;

(p) subsequent to step (o), storing, in a data structure indexed according to a difference between the first and second amounts and also indexed according to one of the data first and second threshold voltages, a count representing the number of times the captured value of step (n) is TRUE during the repeating of steps (a) through (n);

(q) repeating steps (a) through (p) with identically altered values for the first and second data threshold voltages in combination with altered values for the first amount; and

(r) generating an eye diagram from the counts stored in the data structure.

5. An eye diagram analyzer comprising:

a variable clock signal waveform delay circuit having an input for receiving a clock signal and an output producing a delayed clock signal;

a first threshold detector having a variable first threshold, an input for receiving a data signal to be measured as an eye diagram and having an output producing a first logical data signal;

a first variable data signal waveform delay circuit having an input coupled to receive the first logical data signal and an output producing a first delayed logical data signal;

a second threshold detector having a variable second threshold, an input for receiving the data signal to be measured as an eye diagram and having an output producing a second logical data signal;

a second variable data signal waveform delay circuit having an input coupled to receive the second logical data signal and an output producing a second delayed logical data signal;

the first delayed logical data signal and the second logical data signal being delayed by the same amounts;

a transition detection circuit coupled to the delayed clock signal and to the first delayed logical data signal, and having an output producing a transition signal indicative of a transition in the first delayed logical data signal occurring during a selected length of time subsequent to a transition in the delayed clock signal;

a voltage range detection circuit coupled to the delayed clock signal, to the first delayed logical data signal and to the second delayed logical data signal, and having an output producing an in-range detection signal indicative that voltage of the data signal is within a voltage range determined by the first and second thresholds;

a counter coupled to the logical OR of the transition signal with the in-range detection signal, and that counts occurrences thereof; and

a memory whose content is organized as a data structure indexed by the difference in delays for the variable clock signal waveform delay circuit and the variable data signal waveform delay circuit, by at least one of the variable first and second thresholds, and that stores in an indexed location the number of counted occurrences.

6. An eye diagram analyzer comprising:

a variable clock signal waveform delay circuit having an input for receiving a clock signal and an output producing a delayed clock signal;

a first threshold detector having a variable first threshold, an input for receiving a data signal to be measured as an eye diagram and having an output producing a first logical data signal;

a first variable data signal waveform delay circuit having an input coupled to receive the first logical data signal and an output producing a first delayed logical data signal;

a second threshold detector having a variable second threshold, an input for receiving the data signal to be measured as an eye diagram and having an output producing a second logical data signal;

a second variable data signal waveform delay circuit having an input coupled to receive the second logical data signal and an output producing a second delayed logical data signal;

the first delayed logical data signal and the second logical data signal being delayed by selected amounts that de-skew them;

a transition detection circuit coupled to the delayed clock signal and to the first delayed logical data signal, and having an output producing a transition signal indicative of a transition in the first delayed logical data signal occurring during a selected length of time subsequent to a transition in the delayed clock signal;

a voltage range detection circuit coupled to the delayed clock signal, to the first delayed logical data signal and to the second delayed logical data signal, and having an output producing an in-range detection signal indicative that voltage of the data signal is within a voltage range determined by the first and second thresholds;

a counter coupled to the logical OR of the transition signal with the in-range detection signal, and that counts occurrences thereof; and

a memory whose content is organized as a data structure indexed by the difference in delays for the variable clock signal waveform delay circuit and the variable data signal

waveform delay circuit, by the at least one of the variable first and second thresholds, and that stores in an indexed location the number of counted occurrences.